

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): En-Sing Chen, et al.

Title: NAND MEMORY ARRAY INCORPORATING CAPACITANCE  
BOOSTING OF CHANNEL REGIONS IN UNSELECTED MEMORY  
CELLS AND METHOD FOR OPERATION OF SAME

Application No.: 10/729,831

Filed:

December 5, 2003

Examiner: Le, Toan K.

Group Art Unit:

2824

Atty. Docket No.: 023-0028

Confirmation No.:

8528

March 15, 2005

Mail Stop Amendment  
COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450**INFORMATION DISCLOSURE STATEMENT****37 C.F.R. § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the undersigned brings to the Examiner's attention in the above-identified application the patents, publications, applications or other information identified in the attached:

- ☒ Form(s) PTO/SB/08A (5 page(s), with copy of 4 reference(s)).
- ☒ Form(s) PTO/SB/08B (2 page(s), with copy of 20 reference(s)).
- ☒ Listing of Pending Applications (1 page(s), with copy of no application(s)).
- ☐ Other: N/A

Citation of such information shall not be construed as (i) an admission that the information necessarily is, or corresponds to, prior art with respect to the instant invention, (ii) a representation that a search has been made, other than as described herein, or (iii) an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

For each item of information listed that is not in the English language, the undersigned has provided a concise explanation of the relevance through (i) an English language abstract, (ii) an English language equivalent application, or (iii) if cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action that indicates the degree of relevance found by the foreign office.

CERTAIN COPIES NOT INCLUDED

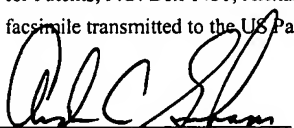
Pursuant to operative regulations, certain copies need not be provided and corresponding information is identified in this Information Disclosure Statement by citation only. In particular,

- ☒ In accordance with 37 C.F.R. § 1.98(a)(2)(ii), copies of cited U.S. Patents and U.S. Patent Application Publications are not included.
- ☐ Certain information was submitted to, or cited by, the Office in Application No(s). N/A, filed N/A, to which the above-identified application claims priority under 35 U.S.C. § 120. In accordance with 37 C.F.R. § 1.98(d), copies of that information are not included.
- ☒ Pursuant to 1287 OG 163 (October 19, 2004), for those cited pending U.S. patent applications filed (or which entered the national stage under 35 U.S.C. § 371) on or after June 30, 2003 or which are otherwise stored in the USPTO's Image File Wrapper system, copies are not included.

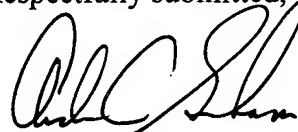
FEE AUTHORIZATION

- ☐ This Information Disclosure Statement is filed within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) or within three months of entry of the national stage as set forth in § 1.491 in an international application. Therefore, no fee is required.
- ☒ The undersigned believes that this Information Disclosure Statement is being filed before the mailing date of a first Office action on the merits or before the mailing date of a first Office action after the filing of a request for continued examination under § 1.114. Therefore, no fee is believed required.

If however, this Information Disclosure Statement is filed after the period specified in § 1.97(b), the undersigned hereby authorizes the Commissioner to charge the fee set forth in § 1.17(p) to Deposit Account No. 50-0631.

<u>CERTIFICATE OF MAILING OR TRANSMISSION</u>	
I hereby certify that, on the date shown below, this correspondence is being	
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	<u>3-15-05</u>
Andrew C. Graham	Date

Respectfully submitted,



Andrew C. Graham, Reg. No. 36,531  
 Attorney for Applicant(s)  
 (512) 338-6313  
 (512) 338-6301 (fax)

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PTO/SB/08A (Substitute for form 1449/PTO)		Attorney Docket No.: 023-0028
		Application No.: 10/729,831
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		First Named Inventor: En-Hsing Chen et al.
		Filing Date: December 5, 2003
		Group Art Unit: 2824
		Examiner Name: Toan K. Le
Sheet 1 of 5		Date Submitted: March 15, 2005



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number-Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
	AA	4,142,176	02-27-1979	Dozier		
	AB	4,543,594	09-24-1985	Mohsen et al.		
	AC	4,602,354	07-22-1986	Craycraft et al.		
	AD	4,868,616	09-19-1989	Johnson et al.		
	AE	5,197,027	03-23-1993	Challa		
	AF	5,301,144	04-05-1994	Kohno		
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	AH	5,429,968	07-04-1995	Koyama		
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	AJ	5,568,421	10-22-1996	Aritome		
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	AL	5,644,533	07-01-1997	Lancaster et al.		
	AM	5,703,382	12-30-1997	Hack et al.		
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
	AN	JA 62-142363	06-25-1987			
	AO	JA 62-155568	07-10-1987			
	AP	JA-2001-358237	12-26-2001			
	AQ	JA-2002-280467	09-27-2002			
Examiner Signature		Examiner Signature		Date Considered		

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional).

<sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04.

<sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3)

<sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

<sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.

<sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08A (Substitute for form 1449/PTO)		Attorney Docket No.: 023-0028
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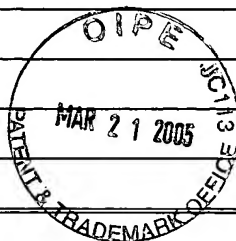
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	AR	5,715,194	02-03-1998	Hu	
	AS	5,751,012	05-12-1998	Wolstenholme et al.	
	AT	5,814,853	09-29-1998	Chen	
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	BD	6,185,122 B1	02-06-2001	Johnson et al.	

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	BE					
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	BI	6,188,611 B1	02-13-2001	Endoh et al.	
	BJ	6,291,836	09-18-2001	Kramer et al.	
	BK	6,307,807 B1	10-23-2001	Sakui et al.	
	BL	6,326,269 B1	12-04-2001	Jeng et al.	
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	BU	6,512,703 B2	01-28-2003	Sakui et al.	

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	BZ	6,515,888	02-04-2003	Johnson et al.	
	CA	6,545,898	04-08-2003	Scheuerlein	
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	CD	6,611,453	08-26-2003	Ning	
	CE	6,614,688 B2	09-02-2003	Jeong et al.	
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	CG	6,621,743 B2	09-16-2003	Ogane	
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	CL	US RE. 35,838	07-07-1998	Momodomi et al.	

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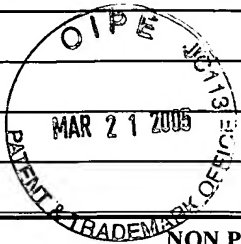
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	CQ	US-2002/0021587 A1.	02-21-2002	Sakui et al	
	CR	US-2002/0028541 A2	03-07-2002	Lee et al.	
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	CT	US-2004/0124415	07-01-2004	Walker et al.	
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	CY	US-6,049,494	04-2000	Sakui et al.	
	CZ	US-5,991,202	11-1999	Derhacopian et al.	
	DA	US-5,812,457	09-1998	Arase	
	DB				
	DC				

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AA	DURISETY, CHANDRA SEKHAR ACHARYULU, "Analysis and Characterization of Single-Poly Floating Gate Devices in 0.35um PDSOI Process", A Thesis Presented for the Master of Science Degree, The University of Tennessee, Knoxville, December 2002, pp. i-viii and 1-80.	
	AB	EVANS, ROBERT J., ET AL., "Energy Consumption Modeling and Optimization for SRAM's," IEEE Journal of Solid-State Circuits, Vol. 30, No. 5, May 1995, pp. 571-579.	
	AC	JUNG, TAE-SUNG, ET AL., "A 117-mm <sup>2</sup> 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1575-1583.	
	AD	KAWAGOE, HIROTO, ET AL., "Minimum Size ROM Structure Compatible with Silicon-Gate E/D MOS LSI," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3, June 1976, pp. 360-364.	
	AE	KIM, KYU-HYOUN, ET AL., "An 8-Bit-Resolution, 360-μs Write Time Nonvolatile Analog Memory Based on Differentially Balanced Constant-Tunneling-Current Scheme (DBCS)," IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, November 1998, pp. 1758-1762.	
	AF	KIM, BYUNGCHEUL, ET AL., "A Scaled SONOS Single-Transistor Memory Cell for a High-Density NOR Structure with Common Source Lines," Journal of the Korean Physical Society, Vol. 41, No. 6, December 2002, pp. 945-948.	
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	AH	KITANO, YOSHITAKA, ET AL., "A 4-Mbit Full-Wafer ROM," IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 4, August 1980, pp. 686-693.	
	AI	LEE, YONG KYU, ET AL., "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI," IEEE Electron Device Letters, Vol. 23, No. 11, November 2002, pp. 664-666.	
	AJ	LIN, HORNG-CHIH, ET AL., "Ambipolar Schottky-Barrier TFTs," IEEE Transactions on Electron Devices, Vol. 49, No. 2, February 2002, pp. 264-270.	
	AK	NAJEEB-UD-DIN ET AL., "Analysis of Floating Body Effects in Thin Film Conventional and Single Pocket SOI MOSFETs Using the GIDL Current Technique", IEEE Electron Device Letters, Vol. 23, No. 4, April 2002, pp. 209-211.	
	AL	NISHIHARA, TOSHIYUKI, ET AL., "A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1479-1484.	
	AM	PARK, KI-TAE, "Recent Non-Volatile Memory Device & Circuit Technology," Halo LSI Inc, (date unknown), 35 pages.	
	AN	ROIZIN, YAKOV, ET AL., "Plasma-Induced Charging in Two Bit per Cell SONOS Memories," Tower Semiconductor Ltd., Migdal HaEmek 23105, Israel, (date unknown), 4 pages.	

Examiner Signature		Date Considered	
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup>Applicant's unique citation designation number (optional).

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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AO	SHIN, JONGSHIN, ET AL., "A New Charge Pump Without Degradation in Threshold Voltage Due to Body Effect," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1227-1230.	
	AP	STURM, J. C., ET AL., "Leakage Current Modeling of Series-Connected Thin Film Transistors," IEEE Transactions on Electron Devices, Vol. 42, No. 8, August 1995, pp. 1561-1563.	
	AQ	SUGIBAYASHI, TADAHICO, ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-1098.	
	AR	SUH, KANG-DEOG, ET AL., "A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1149-1156.	
	AS	TAKEUCHI, KEN, ET AL., "A Negative V <sub>th</sub> Cell Architecture for Highly Scalable, Excellently Noise-Immune, and Highly Reliable NAND Flash Memories," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp. 675-684.	
	AT	THEAN, AARON, ET AL., "Flash memory: towards single-electronics," IEEE Potentials, October/November 2002, pp. 35-41.	
	AU		
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**LIST OF PENDING U. S. PATENT APPLICATIONS**

The following pending U.S. patent applications are listed for consideration by the Examiner.

- 1) U.S. Patent Application No. 10/729,865, filed December 5, 2003, entitled "NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same," naming inventors En-Hsing Chen, Andrew J. Walker, Roy E. Scheuerlein, Sucheta Nallamothe, Alper Ilkbahar, Luca G. Fasoli and James M. Cleeves.
- 2) U.S. Patent Application No. 10/729,844, filed December 5, 2003, entitled "NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same," naming inventors En-Hsing Chen, Andrew J. Walker, Roy E. Scheuerlein, Sucheta Nallamothe, Alper Ilkbahar, and Luca G. Fasoli.
- 3) U.S. Patent Application No. 10/729,843, filed December 5, 2003, entitled "Memory Array Incorporating Memory Cells Arranged in NAND Strings," naming inventors Luca G. Fasoli, Roy E. Scheuerlein, En-Hsing Chen, Sucheta Nallamothe, Maitreyee Mahajani, and Andrew J. Walker.

***Applicant(s) are providing a separate list of pending applications, pursuant to MPEP § 609III(D), to avoid publication of the application numbers on any patent that issues from the above-identified application. Applicant(s) request that the Examiner indicate consideration of the pending applications listed above in accordance with MPEP 609III(C)(2) and return a copy of this page with the next communication.***